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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,218	07/14/2006	Erik J. Marinissen	NL04 0065 US1	2749

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
04/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/586,218	MARINISSEN ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/8/2009 has been entered.

The present Application No. 10/586,218, filed 07/14/2006 is a national stage of PCT/IB05/50153, international Filing Date 01/13/2005, claims foreign priority to EPO Application No. 04100141.3, filed 01/19/2004.

This is a non-Final Office Action in response to the AMENDMENT and RCE filed 4/8/2009. Claims 1-25 are presently under examination and pending.

Response to Arguments

Applicant's arguments in the remarks filed on 4/8/2009, with respect to the rejection of Claim 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Bhattacharya (US Patent No. 6,378,090), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as set forth in the present Office Action, below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-4, 8, 13, 14-17, 20, 22, the limitation "its associated module" renders the claims indefinite, because the limitation fails to clearly define the test wrapper or the global enable signal with which the module is associated. The limitation lacks antecedent basis, and should be amended accordingly, "the module associated with the test wrapper", "the module associated with the control circuit", where ever applicable.

Claims 1, 14, the limitation "whether or not the global enable signal is passed to its associated module" renders the claims indefinite, because the expression "whether or not" is written in the alternative form, thus failing to positively define the active state of the logic circuit. The limitation should be amended accordingly to more clearly define the active state, since patentable weigh is not given to a negative limitation, i.e, the non-active state.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by O'Brien (US Patent No. 6,886,110) filed, August 2, 2001.

Regarding independent Claims 1, 13, O'Brien discloses a JTAG, IEEE 1149.1, Test Access Port and Boundary-Scan Architecture, for testing modules devices (30, 30', 30") connected in series in an electronic circuit, each of the devices including a serial boundary-scan register (Boundary Scan) 84 having boundary-scan cells 44 directly coupled to each device primary input and primary output pin (not shown) interconnected internally that provides switching functionality between functional access (normal mode) and test access (test mode) to core logic 46, Figs. 3-6, the Scan Architecture comprising:

a test access mechanism (scan path 62, Fig. 5) arranged to transport test stimulus data (TDI input 64) to device 30 and to transport test response data (TDO output 66) from device 30" during the test mode (TMS), the scan path 62 is configured to transport the (TDI input 64) and the (TDO output 66) via a single data path that passes through each devices (30, 30', 30") connected in series via the scan path 62, as shown in Fig. 5.

A global enable signal "Test Mode Select" (TMS) on control line 100 coupled to each of the devices (30, 30', 30"), the TMS placing the devices (30, 30', 30") in the test mode. As shown in Fig. 5, step 1, connecting the IRs 88 (FIG. 3) of all three devices between their respective TDI 48 and TDO 50 pins. This is achieved by placing a predetermined sequence of values on the TMS control line 100 that is coupled in parallel to the TAP controller 86 of each device 30, 30', 30".

A plurality of control circuits (TAP controllers 86), each embedded in each of the devices (30, 30', 30") and arranged to place each of the corresponding devices 30, 30', 30" in the (TMS) test mode.

As shown in the example of Fig. 5, IR 88 (FIG. 3) places device 30 (the first device in the chain) into bypass mode (to shorten the time it takes to get test stimulus to follow-on devices 30' and 30") and places devices 30' and 30" into Extest mode preparatory to setting up tests to check the interconnect between devices 30' and 30". This example requires loading the Bypass instruction (all-1s) into the IR 88 of device 30, and the Extest instruction (all-0s) into the IRs 88 of devices 30' and 30".

Referring now to Figs. 7B and 7B, as shown, emulator 110 includes a topology module 171 configured to obtain 172 the topology of the scan chain, and a selection module 175 configured to select 176 one device within the scan chain. A bypass module 181 is configured to place 182 at least one other device within the scan chain into bypass 15 mode. An emulation instruction module 187 is also included, to send 188 (FIG. 7B) emulation instructions to the scan chain, so that the emulation instructions bypass the unselected device(s) and are executed by the selected device.

Regarding Claims 2-12, 24-25, O'Brien discloses in Fig. 5,

Step 1 connects the IRs 88 (Fig. 3) of all three devices between their respective TDI 48 and TDO 50 pins. This is achieved by placing a predetermined sequence of values on the TMS control line 100 that is coupled in parallel to the TAP controller 86 of each device 30, 30', 30".

Step 2 loads the appropriate instructions into the various IRs 88 through scan path 62 that now serially connects them to one another. In the event each IR 88 simply contains two-bits, this operation amounts to a serial load of the sequence 110000 into the edge-connector TDI 64 to place 00 in IR 88 of each device 30' and 30", and place 11 in IR 88 of device 30. The IRs 88 are now set up with the correct instructions loaded into their shift sections 94.

Step 3 places values on TMS line 100 to cause each TAP controller 86 to issue control-signal values that transfer the values in the shift sections 94 of the IRs 88 to hold sections 96 where they become the "current" instruction. This is the Update operation. At this point, the various instructions are obeyed--that is, device 30 deselects its IR 88 and selects its Bypass register 90 between its TDI 48 and TDO 50 (i.e., to execute its Bypass instruction). Devices 30' and 30" deselect their IRs 88 and select their boundary-scan registers 84 between their TDI 48 and TDO 50 (i.e., to execute their Extest instructions). The devices 30, 30', and 30"are now set up for the Extest operation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/
Primary Examiner, Art Unit 2117

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Office Action: 20090423. Non-Final Rejection

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